IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INNOVATIVE MEMORY SYSTEMS, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., Defendant.	Civil Action No. 1:14-cv-1480-RGA **JURY TRIAL DEMANDED** **REDACTED PUBLIC VERSION**

MICRON TECHNOLOGY, INC.'S OPENING BRIEF IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT

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1	U.S. Patent No. 7,000,063 ("'063 patent")
2	U.S. Patent No. 6,901,498 ("'498 patent")
3	Claim Construction hearing transcript, dated November 3, 2020
4	Excerpts from the Opening Infringement Expert Report of Andrew Wolfe, Ph.D., dated January 5, 2022 [Filed Under Seal]
5	Excerpts from the Expert Report of Joseph C. McAlexander III Regarding Non-Infringement of U.S. Patent Nos. 6,901,498 and 7,000,063, dated February 4, 2022 [Filed Under Seal]
6	Excerpts from the deposition transcript of Andrew Wolfe, Ph.D, taken on March 10, 2022 [Filed Under Seal]
7	Excerpts from the Reply Report of Andrew Wolfe, Ph.D. Regarding Infringement, dated February 23, 2022 [Filed Under Seal]
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9	JPH06274656A ("Eiichi") (MIMS-PA0011473)
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11	Excerpts from the deposition transcript of Kevin Kilbuck, taken on November 2, 2021 [Filed Under Seal]
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I. NATURE AND STAGE OF PROCEEDINGS

This is a patent case brought by Innovative Memory Systems, Inc. ("IMS") against Micron Technology, Inc. ("Micron"). Only two patents are left in the case: U.S. Patent Nos. 7,000,063 (Ex. 1[1], the "'063 patent") and 6,901,498 (Ex. 2, the "'498 patent," and collectively "the Asserted Patents"). The Court has construed the claims of the Asserted Patents. D.I. 154. Expert discovery has been completed and trial is scheduled for September 26, 2022. This is Micron's motion for summary judgment and partial summary judgment.

II. SUMMARY OF ARGUMENT

Micron seeks summary judgment and partial summary judgment related to six different issues. First, the '063 patent is invalid as a matter of law for claiming patent-ineligible subject matter. The Federal Circuit has repeatedly confirmed that a claim "directed to a result or effect that itself is the abstract idea and merely invokes generic processes and machinery" is impermissibly abstract under § 101. *Two-Way Media Ltd. v. Comcast Cable Commc'ns., LLC*, 874 F.3d 1329, 1337 (Fed. Cir. 2017) (citations omitted). There is no dispute that the claims as construed cover the very idea of causing write-many memory cells to become write-once memory cells: IMS told the Court that the claim language does not "specify[] … any particular method of limiting that write, the number of writes to one." Ex. 3 at 17:15-19. Nor is there any other inventive concept or technological improvement recited in the claims.

Second, Micron moves for summary judgment of non-infringement of the '063 patent or, in the alternative, for summary judgment of invalidity. Under the Court's construction, the '063 Asserted Claims require a rendering step that causes write-many memory cells to become "write-once memory cells," *i.e.*, memory cells "that cannot be written to more than once." It is

[1] Exhibits cited throughout are attached to the Declaration of Jason Lang in Support of Micron's Opening Brief in Support of its Motion for Summary Judgment filed concurrently herewith.

undisputed, however, that the accused "write-once memory cells" are always capable of being written to more than once (and are) in a particular mode of operation, namely, test mode. Because the claims are not limited to a particular operating mode, *e.g.*, "cannot be written to more than once [outside of test mode]," the accused products cannot infringe. If the Court were to reconstrue "write-once memory cells" to exclude subsequent writes in test mode, the asserted '063 claims are invalid. Under such a construction, IMS effectively concedes that Japanese Patent Application Publication No. H6-274656 ("Eiichi") discloses rendering write-many memory cells into write-once memory cells.

Third, Micron moves for summary judgment of non-infringement of the '498 patent. As construed, all Asserted Claims require shifting of "assigned blocks," *i.e.*, blocks that have an assigned logical address, "from one logical zone" to another. It is undisputed that Micron's blocks are neither "assigned" nor part of a "logical zone" when transferred to another zone.

Fourth, Micron moves for partial summary judgment that IMS's pre-notice damages for the '498 patent are barred by its failure to mark. Micron met its initial burden of identifying pre-suit products sold by the patentee that are relevant to the '498 patent, shifting the burden to IMS to show that the products need not be marked. IMS and its expert have instead pleaded ignorance of these products and, as such, have provided no evidence to carry their burden.

Fifth, Micron moves for partial summary judgment that IMS may not recover damages for accused products that are neither made, used, sold or offered for sale in the U.S., or imported into the U.S. One of IMS's damages theories seeks to recover for all of Micron's sales anywhere in the world. However, IMS cannot show that all of those accused products are tied to allegedly infringing activity in the U.S. Because IMS has no other basis for obtaining damages on worldwide sales, partial summary judgment is warranted.

Sixth, Micron moves for partial summary judgment that IMS may not hold Micron liable for the allegedly infringing acts of its non-party subsidiaries. IMS has never pleaded or disclosed such a theory. Further, IMS cannot meet its burden to show that Micron's non-party subsidiaries are its "alter egos" or that Micron "instigates" them to allegedly infringe as its agent.

III. THE '063 PATENT IS INVALID UNDER SECTION 101

A. The Law Of Patent Ineligibility

"Whether a claim is drawn to patent-eligible subject matter under § 101 is a threshold inquiry." *In re Bilski*, 545 F.3d 943, 950 (Fed. Cir. 2008), *aff'd, Bilski v. Kappos*, 561 U.S. 593, 602 (2010) (describing § 101 as "a threshold test"). Where, as here, no potentially disputed facts are material to the outcome, summary judgment is appropriate. *See Innovation Scis., LLC v. Amazon.com Inc.*, 778 F. App'x 859, 864 (Fed. Cir. 2019) (finding no disputed facts when result-oriented claim sought to "capture the broad concept… rather than a specific way to do so.")

The Supreme Court has set forth a two-part test for determining whether a patent recites ineligible subject matter. *Alice Corp. PTY. Ltd v. CLS Bank Int'l*, 573 U.S. 208, 217-18 (2014). The first step considers the "focus of the claimed advance over the prior art to determine if the claim's character as a whole is directed to excluded subject matter." *Affinity Labs of Texas, LLC v. DirecTV, LLC*, 838 F.3d 1253, 1257 (Fed. Cir. 2016) (quotations omitted). Courts assessing abstractness examine whether the claims "focus on a specific means or method, or are instead directed to a result or effect that itself is the abstract idea and merely invokes generic processes and machinery." *Two-Way Media*, 874 F.3d at 1337.

If the claim is directed to an abstract idea, the Court proceeds to step two and asks whether the claim elements, considered "both individually and 'as an ordered combination,'" recite an "inventive concept" that is "sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [abstract idea] itself." *Alice*, 573 U.S. at 217-18.

B. The Asserted Claims Are Abstract Under The First Step Of *Alice*

1. The Asserted Claims are directed to the abstract idea causing write-many memory cells to become write-once memory cells.

The '063 patent is "directed to" the idea of causing write-many memory cells to become write-once memory cells. This concept is the clear "focus" of the Asserted Claims. *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 765 (Fed. Cir. 2019) (citing *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353(Fed. Cir. 2016)). Claim 42, the only asserted independent claim, reads:

> 42. A method for creating a write-once memory device from a write-many memory device, the method comprising:
>
> > (a) providing a memory device comprising a memory array comprising a plurality of write-many memory cell [sic]; and
> >
> > (b) rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells.[2]

Claim 42 thus recites only two steps, generally requiring (1) "providing" a memory device with write-many memory cells and (2) "rendering" some of those cells into write-once memory cells. IMS's counsel has admitted the same, arguing during the Markman hearing that "the invention is directed to simply limiting the number of writes to a write-many memory cell in a memory device." Ex. 3 at 17:12-14. The specification confirms this focus, explaining that limiting the number of writes was "the problem facing the inventor." *ChargePoint,* 920 F.3d at 767. Specifically, the '063 patent explains (inaccurately) that "[c]urrently, there are no write-

[2] Claims 43 and 44 are also asserted, but add only minor details. Claim 43 adds that the claimed memory device must be removably couplable with a host device. Claim 44 adds that the "rendering" step of claim 42 be performed by a "manufacturer" of the memory. These additional limitations do not change the fact that the "character as a whole" of each of the Asserted Claims is about taking write-many memory cells and causing them to become write-once memory cells. *Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343, 1346 (Fed. Cir. 2015).

many devices that control the number of allowable writes (or re-writes) to the memory device." '063 patent at 1:12-14.

This "focus" renders the claims abstract at step one because instead of claiming a solution to that problem, they recite the very idea of solving the problem. "Indeed, the essentially result-focused, functional character of claim language has been a frequent feature of claims held ineligible under § 101." *Elec. Power Grp.,* 830 F.3d at 1356; *see also Apple, Inc. v. Ameranth, Inc.*, 842 F.3d 1229, 1244 (Fed. Cir. 2016) ("Generally, a claim that merely describes an effect or result dissociated from any method by which it is accomplished is not directed to patent-eligible subject matter.") (citations and quotation marks omitted). Such claims are impermissibly abstract because they are "drafted in such a result-oriented way that they amounted to encompassing the 'principle in the abstract' no matter how implemented." *Interval Licensing LLC v. AOL, Inc.*, 896 F.3d 1335, 1343 (Fed. Cir. 2018).

Time after time, the Federal Circuit has affirmed that claims directed to a result with no limitation as to *how* the result is achieved are abstract at step one. In *Affinity Labs*, the court confirmed that claims directed to "providing out-of-region access to regional broadcast content" were abstract because the claims merely recited "the function of wirelessly communicating regional broadcast content to an out-of-region recipient, not a particular way of performing that function." 838 F.3d at 1258. In *Two-Way Media*, the Federal Circuit affirmed that a claim concerning the delivery of message packets was abstract because it merely "recite[d] a method for routing information using result-based functional language" and did "not sufficiently describe how to achieve these results in a non-abstract way." 874 F.3d at 1337. In *Electric Power Group,* the Federal Circuit found a claim directed to the result of "detecting events on an interconnected electric power grid in real time" to be abstract, noting that "there is a critical difference between

patenting a particular concrete solution to a problem and attempting to patent the abstract idea of a solution to the problem in general." 830 F.3d at 1351, 1356 (citing district court). Yet again, in *Dropbox, Inc. v. Synchronoss Techs., Inc.*, the Federal Circuit affirmed that a claim directed to a data security device was abstract because "[t]he claim does not provide any limits that curb how the apparatus performs these functions." 815 F. App'x 529, 532 (Fed. Cir. 2020).

This Court too has confirmed that result-oriented claims are abstract under the first step of *Alice*. In *B# On Demand LLC v. Spotify Tech. S.A.*, the Court held that claims relating to distributing media according to certain rules were abstract because "[t]he claims use a wholly generic computer system to obtain functional results of limiting access to distributed media based on predetermined rules with no technical detail describing how to achieve those results." 484 F.Supp.3d 188, 203 (D. Del. 2020).

Here, under the Court's claim construction, the Asserted Claims are directed to a result rather than any specific technique for obtaining that result. The Asserted Claims covers any and all ways of "causing at least some of the write many memory cells in the memory array to become write-once memory cells." D.I. 154 at 2; *see also Am. Axle & Mfg., Inc. v. Neapco Holdings LLC*, 967 F.3d 1285, 1295 (Fed. Cir. 2019) (finding claims ineligible that recited "simply the concept of achieving [a] result, by whatever structures or steps happen to work"). Like the claims found to be impermissibly abstract in *Affinity Labs*, *Two-Way Media*, *Dropbox, B# On Demand*, and many others, claim 42 says nothing about <u>how</u> that result is achieved. This is by IMS's design, because it argued during claim construction that claim 42 recites "limiting the number of writes to a write-many memory device in the memory array to one write, again, <u>without specifying in the claim language any particular method</u> of limiting that write, the number of writes to one." Ex. 3, Markman Hearing Tr., 17:16-19 (emphasis added). IMS's counsel

further argued that the claims recite "*[n]othing about specifically how* you limit the number of writes to N number of writes," adding that "*there is nothing in the clear and unambiguous language that says anything about how* you must [limit the number of writes to one]." *Id.*, 24:7-9, 20-21 (emphasis added). The Court's construction, and IMS's admissions, both establish that the claims lack "the specificity required to transform a claim from one claiming only a result to one claiming a way of achieving it." *SAP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1167 (Fed. Cir. 2018).[3]

2. The Asserted Claims are not directed to a specific improvement to the way computers operate.

The Asserted Claims also are abstract as a matter of law because they fail to recite any "specific improvement to the way computers operate." *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1336 (Fed. Cir. 2016). In its opposition to Micron's previously filed motion on the pleadings, IMS argued that claim 42 was actually directed to a "technological improvement to conventional write-many memory devices." D.I. 174 at 13. It is not.

Because the Asserted Claims recite nothing more than a result, they cannot be directed to a specific improvement to the way computers operate. As the Federal Circuit has explained, reciting "the mere *function*" of achieving the claimed result "is not a specific improvement to the way computers operate." *Univ. of Fla. Research Found., Inc. v. Gen. Elec. Co.*, 916 F.3d 1363, 1368 (Fed. Cir. 2019) (emphasis in original and citations omitted). Rather, "[t]o claim a technological solution to a technological problem, the patent must actually *claim* the

[3] To the extent that IMS argues that result-oriented claiming only leads to abstraction when the claims recite a "software" invention, it is incorrect. First, numerous cases have held non-software result-oriented claims to be abstract. *See, e.g.*, *Elec. Power Grp.*, 830 F.3d at 1353 (power grid monitoring); *ChargePoint*, 920 F.3d at 772-73 (network-enabled electric vehicle chargers); *Am. Axle & Mfg.*, 967 F.3d at 1292-98 (manufacture of driveline shaft assembly). Second, the Asserted Claims are so untethered to any implementation that they in fact do encompass generic software methods for achieving the claimed "rendering."

technological solution." *Dropbox*, 815 F. App'x at 535 (emphasis in original). The Asserted Claims recite no such improvement or solution, instead claiming the very *idea* of converting write-many memory cells to write-once memory cells. *See cxLoyalty, Inc. v. Maritz Holdings Inc.*, 986 F.3d 1367, 1379 (Fed. Cir. 2021) (disagreeing that claims resulted in improved computer functioning when the claims did not "provide any guidance as to how this purported function is achieved").

The Federal Circuit rejected similar arguments in *Free Stream Media Corp. v. Alphonso Inc.*, 996 F.3d 1355 (Fed. Cir. 2021). There, the patentee argued that claims directed to providing tailored advertisements based on television viewing habits were not abstract because they resulted in a "specific asserted improvement in computer capabilities." *Id.* at 1362. But the Federal Circuit rejected the patentee's contention that the claims beneficially "allow[ed] devices on the same network to communicate where such devices were previously unable to do so" because the "claims do not at all describe how that result is achieved." *Id.* at 1363-34. The court likewise found that the specification failed to change the outcome because "[t]he asserted claims do not incorporate" disclosures for achieving the claimed result. *Id.* at 1354. Because the Asserted Claims here likewise fail to recite any details as to *how* one achieves the claimed result, they likewise fail to recite any specific improvement to the way computers operate. *See B# On Demand*, 484 F.Supp.3d at 203 (finding no technical improvement where "[t]he claims use[d] a wholly generic computer system to obtain functional results" and included "no technical detail describing how to achieve those results"). Thus, even if IMS asserts that benefits are obtained when one renders write-many memory cells into write-once memory cells, those alleged benefits cannot save the '063 patent because the Asserted Claims lack any specific way of achieving an improvement. *See Chargepoint*, 920 F.3d at 769-770 (Fed. Cir. 2019) (finding that a "result-

oriented" claim to a "good idea" was nonetheless abstract under step one).

C. The Asserted Claims Lack Any Inventive Concept.

The Asserted Claims lack an inventive concept "sufficient to ensure that the patent in practice amounts to significantly more than" an attempt to patent the abstract idea itself. *Alice*, 573 U.S. at 218 (citations omitted). Examining the claim limitations both individually and as an ordered combination makes clear that the Asserted Claims recite nothing more than the abstract idea of causing write-many memory cells to become write-once memory cells.

It is well established that reciting "the use of generic features" and "routine functions" to "to implement the underlying idea" does not supply a claim with an inventive concept. *Affinity Labs*, 838 F.3d at 1262. Here, the Asserted Claims does not even go that far. They do not recite *any way* of implementing the underlying idea *at all*. As such, the claims cover all ways, including wholly generic and routine ways, of causing write-many memory cells to become write-once memory cells. Even at its most specific, the patent simply invokes basic and conventional programming functions like counting writes and setting variables, both of which IMS has admitted were conventional and well-known programming techniques, and both of which fall within the result-oriented scope of the claims. Ex. 3 at 33:19-20 ("Setting N to 1, setting a variable to one, that was known in other contexts.") 34:4-7 ("Certainly people knew how to understand how many – to know how many times a memory cell had been written to. There was nothing novel about that."). And as the Court acknowledged, the parties agree that claim 42 "does not recite something technologically difficult" and one of ordinary skill in the art "would not have had any issue limiting the number of writes to a memory cell." D.I. 149 at 11. As such, the result-oriented breadth of the claims encompasses implementing the abstract idea using only "well-understood, routine, conventional activities previously known to the industry." *Alice*, 573 U.S. 208, 225 (internal quotations and modifications omitted).

Examining claim 42's limitations as "an ordered combination" likewise provides no inventive concept. Claim 42 is short. The first step of claim 42 sets forth a memory device with write-many memory cells, and the second step just requires changing some of the write-many cells in that device to write-once cells. There is nothing else to the claim, and "[i]t has been clear since *Alice* that a claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept that renders the invention 'significantly more' than that ineligible concept." *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1290 (Fed. Cir. 2018).

The two asserted dependent claims fail to add any inventive concept to claim 42. Dependent claim 43 simply requires that the memory device be removable, which IMS has read broadly to cover a packaged memory chip. Ex. 4 ¶ 257. This insignificant limitation adds no clarity regarding "how" the rendering occurs. Claim 44 only requires that the "manufacturer" be the actor that performs the claimed rendering. In other words, this limitation only specifies *who performs* the abstract method, and allows virtually anyone to do so among the broad group of actors that would conventionally be responsible for programming memory devices.[4] These dependent claims in no way "transform the claimed abstract idea into a patent-eligible application." *Alice*, 573 U.S. at 221 (citations and internal quotations marks omitted).

IV. THE ACCUSED PRODUCTS DO NOT INFRINGE THE '063 PATENT OR, ALTERNATIVELY, THE '063 PATENT'S ASSERTED CLAIMS ARE INVALID OVER EIICHI.

IMS asserts claims 42-44 of the '063 patent against Micron's manufacturing of NAND Flash memory products that include a One-Time Programmable ("OTP") area (collectively, "the '063 Accused Products"). Ex. 4 ¶ 205. Under the Court's claim construction, the claims require

[4] The '063 patent and the parties' stipulated construction defines "manufacturer" broadly as "any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging, sale or distribution of the memory device." D.I. 154 at 1; *see also* '063 patent at 3:61-67 (reciting similar definition).

that the "write-once memory cells" "cannot be written to more than once." D.I. 154 at 1. As explained below, Micron's manufacture of the accused OTP area cannot infringe because it is undisputed that the accused "write-once memory cells," *i.e.*, the OTP memory cells, can be (and are) ***written to more than once***. Contrary to IMS's argument, it does not matter under the claim language, the Court's construction, or Federal Circuit precedent that this capability to write the cells more than once resides in a Micron test mode.

If this Court allows IMS to rewrite the Court's construction to be "memory cells that cannot be written to more than once [except in test mode]," then Micron is entitled to summary judgment of invalidity because the Asserted Claims would be invalid in view of the Eiichi prior art reference. There is no genuine dispute that, under this revised construction, Eiichi discloses converting write-many memory cells into to write-once memory cells.

A. Overview Of The '063 Accused Products

During manufacturing of the '063 Accused Products, an area of the memory is designated as the OTP area. Ex. A ¶ 41. Micron's products operate in various modes. It is undisputed that in one mode (a test mode), the OTP area may be erased and written to as many times as one desires. Ex. 4 ¶ 225; Ex. 6 at 151:6-17, 161:16-23, 169:2-16, 181:17-182:5, 249:21-250:4; *see also* Ex. A ¶¶ 42-45. In a different mode (an OTP operation mode), the memory cells cannot be erased. IMS contends that in this mode, writes to the OTP area are limited to one and the OTP area comprises "write-once memory cells." Ex. 4 ¶¶ 206, 230, 245.

B. The '063 Accused Products Do Not Infringe Claims 42-44.

Claim 42 is an independent claim that recites "rendering at least some of the write-many memory cells in the memory array as write-once memory cells by preventing more than one write to said at least some of the write-many memory cells." The Court construed this limitation to mean: "causing at least some of the write-many memory cells in the memory array to become

write-once memory cells." D.I. 154 at 2. In adopting this construction, the Court referenced the parties' agreed-upon construction of "write-once memory cells," which is "memory cells that cannot be written to more than once." D.I. 149 at 11; D.I. 154 at 1-2. Under the Court's construction, Micron's manufacture of the '063 Accused Products cannot infringe claims 42-44 as a matter of law because the alleged "write-once memory cells," *i.e.*, the OTP memory cells, can be (and are) written to "more than once."

[redacted] In other words, IMS admits that the OTP memory cells that allegedly "cannot be written to more than once" are capable of being written to more than once. *Id.* What's more, this is no mere hypothetical capability. After the OTP cells allegedly become "write-once memory cells," IMS admits that the memory cells are written to *again* by Micron [redacted] and will be *further written to* by a customer. Ex. 6 at 157:12-16, 159:23-160:15; Ex. 4 ¶ 206; Ex. 7 ¶ 49. Thus, after the creation of the OTP cells that allegedly "cannot be written to more than once," IMS admits that the OTP cells are written to at least twice. *Id.*

IMS asserts that Micron nonetheless infringes because [redacted] Ex. 4 ¶¶ 206, 213, 216, 225, 246.

This argument cannot avoid summary judgment.

First, the argument ignores the Court's claim construction. The Court construed write-once memory cells to mean memory cells that "cannot be written to more than once"—not "cannot be written to more than once [by a customer]" or "cannot be written to more than once [outside of test mode]." D.I. 154 at 1. In other words, the Court's construction does not include any exception to the requirement that once rendered, the memory cells cannot be written to more than once. *Id.* at 1-2. Indeed, modifying the Court's construction to include any such exception would be improper. *See Integra Lifesciences Corp. v. HyperBranch Med. Tech., Inc.*, No. 15-819-LPS-CJB, 2018 WL 1785033, *5 (D. Del. Apr. 4, 2018) (striking an expert's opinion that modified the court's claim construction by adding additional limitations to the construction).

Second, Federal Circuit precedent holds that a claim limitation applies to all modes of operation unless the claim says otherwise. In *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, the Federal Circuit ruled that a claim limitation requiring that "a variable current limit threshold that increases during … on time" was met by a prior art device that only did so while not in "normal operation." 843 F.3d 1315, 1336-38 (Fed. Cir. 2016). There, like here, nothing in the claim language limited its scope to "normal operation" or "normal conditions." *Id.* What's more, t[redacted] Accordingly, IMS cannot focus on certain modes to the exclusion of others to argue that Micron's OTP cells "cannot be written to more than once."

Although [redacted] demonstrates that Micron's memory cells are never rendered as "write-once memory cells," IMS argues that the "rendering" occurs when [redacted] is an irrelevant step

that merely "unrenders" the memory cells back to write-many memory cells. *See, e.g.*, Ex. 6 at 156:8-17; Ex. 7 ¶ 49. This argument, which ignores the plain meaning of the Court's claim construction, cannot avoid summary judgment. The Court's construction limits "write-once memory cells" to "memory cells that cannot be written to more than once." D.I. 154 at 1. If memory cells are designed so that they can be "unrendered," and thus written to more than once, then those cells were never "memory cells that cannot be written to more than once." Indeed, IMS's expert makes the same argument in attempting to distinguish the prior art. Specifically, for the TrueFFS prior art system, IMS's expert opines that the prior art memory cells were never rendered as write-once memory cells because the device allegedly can be reformatted to allow for further writes. Ex. 8 ¶¶ 183-86. The same reasoning applies to the '063 Accused Products—the fact that they are designed so that the memory cells can be written to more than once demonstrates that they were never "rendered" as "write-once memory cells" in the first place.

C. In The Alternative, Eiichi Renders Claims 42-44 Invalid.

If the Court were to reinterpret "write-once memory cells" to mean memory cells that cannot be written to more than once [redacted], then IMS's concessions establish that the '063 Asserted Claims are anticipated by or obvious in view of Eiichi.

There is no dispute that Eiichi was published on September 30, 1994 and is therefore prior art to the '063 patent under at least 35 U.S.C. § 102(b). Ex. 9; Ex. 10; Ex. 8 ¶ 145 (noting that '063 patent's filing date is October 5, 2001). Additionally, there is no relevant factual dispute about how Eiichi operates. IMS's expert concedes that:

> [Eiichi's] memory is manufactured in an OTP configuration until it is connected, after the device is fabricated, to a tester or similar device and an external test mode signal is provided by the tester. Providing this signal to the device results in a transient write-many state, which has been created from a write-once device, until the signal is removed, at which point the circuit operation resorts back to write-once.

Ex. 8 ¶ 193. This and other concessions show that, under IMS's reinterpretation of the claims, Eiichi's memory device practices claim 42's method for creating a write-once memory device from a write-many memory device.

First, IMS concedes that Eiichi teaches "providing a memory device comprising a memory array comprising a plurality of write-many memory cell [sic]," '063 patent, claim 42. IMS asserts that "Eiichi manufactures its memory devices as write-once memory devices." Ex. 8 ¶ 192. IMS further concedes that when the Eiichi device receives a signal in a "test mode," the device enters "a transient write-many state." *Id.* ¶ 193; *see also* Ex. 10 ¶¶ [0015], [0021], [0046]-[0047]. In other words, upon receiving the signal in test mode, the device becomes a memory device comprising a memory array[5] of memory cells to which data can be written more than once. Ex. 8 ¶¶ 193, 199 (admitting that in test mode, Eiichi's memory device becomes "capable of erasure and rewriting"); *see also* Ex. 10 ¶¶ [0015], [0021], [0046]-[0047].

Second, Eiichi discloses the rendering step of "causing at least some of the write-many memory cells in the memory array to become write-once memory cells," D.I. 154 at 2. IMS concedes that once the test mode "signal is removed…the circuit operation resorts back to write-once." Ex. 8 ¶ 193. In other words, after exiting the test mode, the memory cells to which data can be written more than once in Eiichi's memory device revert to memory cells that cannot be written to more than once (unless one were to re-enter test mode). *Id.*; *see also* Ex. 10 ¶¶ [0011], [0019], [0021]; Ex. A ¶¶ 54-58.

Third, if the preamble is limiting, Eiichi discloses "[a] method for creating a write-once memory device from a write-many memory device," '063 patent, claim 42. IMS concedes that

[5] There is no dispute that Eiichi includes a "memory array," Ex. 10 ¶ [0011] ("matrix" of "memory elements"), or that Eiichi's device is a "memory device" at this point, *id.* ¶¶ [0011], [0017] (the device is "package[d]"). Ex. A ¶¶ 46-49, 51-53.

in test mode, the "device" is in a "write-many state," Ex. 8 ¶¶ 192-93, and that exiting the test mode causes Eiichi's "device" to "resort[] back to write-once," *id.* ¶ 193. This means that exiting test mode causes Eiichi's memory device to become a write-once memory device. *Id.* ¶ 192 ("Eiichi manufactures its memory devices as write-once memory devices."); Ex. A ¶ 50.

IMS does not dispute any of the facts above. Nonetheless, it argues that "[b]ecause Eiichi starts with creating a write-once memory device, it does not meet the limitation of creating a write-once memory device from a write-many memory device that is manufactured to have a plurality of write-many memory cells, some of which are rendered as write-once memory cells." Ex. 8 ¶ 192. This argument fails as a matter of law. Claim 42 is a comprising claim. Thus, as long as Eiichi discloses each of the steps of claim 42, it is legally irrelevant that Eiichi discloses additional steps. *Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1319 (Fed. Cir. 2009) (ruling that the fact that a prior art reference discloses additional steps does not prevent the reference from anticipating a "comprising" method claim). In other words, that Eiichi includes an additional, unrecited step of first creating a write-once memory device is legally irrelevant.

IMS also appears to argue that Eiichi does not anticipate claim 42 because the Eiichi memory device is only a write-many device for a "transient" period of time. Ex. 8 ¶ 193. This argument also fails as a matter of law. It is legally inconsequential that Eiichi's memory device has write-many memory cells only in a "transient" test mode before rendering the write-many memory cells into write-once memory cells. *See Power Integrations*, 843 F.3d at 1336-38 ("[A] prior art product that sometimes, but not always, embodies a claimed method nonetheless teaches that aspect of the invention." (internal quotations omitted)).

In sum, there is no dispute that Eiichi provides a memory device that is only rewritable in test mode. Nor is there any dispute that Eiichi discloses not providing the test mode information

to the user, so that from the customer's perspective, the write-many cells become write-once memory cells. Ex. 10 ¶ [0011]. Under IMS's revised claim construction, the fact that the device could be put back into test mode and written to is irrelevant. If the Court were to embrace IMS's new construction of "write-once memory cells," then Eiichi's memory in a customer's hands includes "write-once memory cells" and anticipates claim 42.

Eiichi also renders claim 43 invalid. Claim 43 depends from claim 42 and adds that the claimed memory device "comprises a modular memory device that is removably couplable [with] a host device." '063 patent, claim 43. First, as IMS's expert admits, a packaged memory chip meets this limitation. Ex. 4 ¶¶ 257-58. Eiichi performs its testing on a packaged device. Ex. 10 ¶¶ [0011], [0017] (testing on "package-sealed state"). Thus, IMS concedes that this additional limitation is met by Eiichi, and Eiichi anticipates claim 43.

Alternatively, Micron's expert opines that a POSITA would have been motivated, with a high expectation of success, to implement Eiichi's memory device in a ***card*** that is removably couplable to a host. Ex. A ¶¶ 59-68. IMS's expert's only rebuttal is that some of the prior art (not addressing Eiichi directly) performs the rendering before packaging. Ex. 8 ¶¶ 273-74. This opinion does not raise a genuine issue, and should be ignored, because it directly contradicts the record: Eiichi expressly discloses its testing (the "rendering") after packaging. Ex. 10 ¶¶ [0011], [0017]. Thus, Eiichi renders claim 43 obvious.

Eiichi also renders claim 44 invalid. Claim 44 depends from claim 42 and adds that "at least some of the write-many memory cells in the memory array are rendered as write-once memory cells by a manufacturer of the memory device." '063 patent, claim 44. The Court construed "manufacturer" as "any party who handles the memory device before it is sold or distributed to an end user, including a party involved in the manufacturing, assembly, packaging,

sale or distribution of the memory device." D.I. 154 at 1. Eiichi discloses that the test mode in which the memory device has "transient" write-many memory cells is "used by the microcomputer manufacturer." Ex. 10 ¶ [0011]. As explained above, once the manufacturer causes the memory device to exit the test mode, the "transient" write-many memory cells in the memory device are reverted to memory cells that cannot be written to more than once (under IMS's new construction). *Id.* ¶¶ [0011], [0019], [0021]; Ex. A ¶¶ 69-70. IMS does not dispute any of these facts. Ex. 8 ¶¶ 188-200. Thus, Eiichi anticipates claim 44.

V. MICRON DOES NOT INFRINGE THE '498 PATENT AS A MATTER OF LAW

Claims 1 and 11 of the '498 patent both require that "the correspondence of blocks to zones is adjustable by controller." Claim 43 similarly requires that "the correspondence between physical blocks and logical address sections is adaptable by the controller in response to defects in the memory." To salvage the '498 patent in IPR proceedings, IMS represented to the Patent Office and the Federal Circuit that these "correspondence" limitations cover only the shifting of "assigned blocks" (*i.e.*, blocks with assigned logical addresses) "from one logical zone" to another logical zone. The Federal Circuit relied on these representations and construed the '498 patent's claims in the manner IMS itself proposed. Later, realizing that the "assigned blocks from one logical zone" requirement was fatal to its infringement case, IMS attempted an about-face in this Court, proposing a claim construction that omitted the "assigned blocks" requirement. D.I. 138, Ex. A, 4. But IMS could not reconcile this position with its prior representations to the Patent Office and Federal Circuit, and this Court construed the claims to require that "the controller can adjust zone boundaries such that ***assigned blocks from one logical zone*** are shifted to another logical zone."[6] D.I. 149 at 11-12 (emphasis added).

[6] There are three independent claims at issue (1, 11, and 43), and each was construed to require this zone adjustment by shifting "assigned blocks." D.I. 154.

Under the Court's construction, IMS cannot prove infringement as a matter of law. Even assuming that blocks are shifted in Micron's products, there is no dispute that at the time of the alleged shifting, the blocks are ***not "assigned blocks"*** (*i.e.*, they do not have assigned logical addresses) and are ***not "from one logical zone"*** (*i.e.*, they are not part of any logical zone). IMS argues that Micron's blocks meet this limitation because [redacted] This argument fails as a matter of law because it is inconsistent with the Court's construction. In fact, it is contrary to statements IMS made both during IPR of the '498 patent and in this case. As such, Micron is entitled to summary judgment of non-infringement.

A. Based On The Court's Claim Construction And The Undisputed Facts, Micron's Products Do Not Infringe

There is no genuine dispute that Micron's products do not infringe under the Court's construction. IMS accuses three Micron products: Micron's MX500, P320h, and P420m products. *See* Ex. 4 ¶ 59. None of these products satisfies the limitations requiring that the "correspondence of blocks to zones" be "adjustable" or "adaptable" by the "controller," because it is undisputed that no "assigned blocks" "from one logical zone" are moved to another. Instead, [redacted]

In connection with the MX500 product, IMS contends that the product operates as described in U.S. Patent No. 8,949,507 (Ex. 12, the "'507 patent"). IMS points to the '507 patent's "meta blocks" as the claimed "logical zones." *See* Ex. 4 ¶ 167. Each meta block includes a collection of blocks. *See id.* When a block in a meta block fails, that meta block is retired and any remaining good blocks within the meta block are listed in a spare block table.

See id. ¶¶ 139-44. Then, if a block in another meta block fails, these spare blocks can replace this failing block. *See id.; see also* '507 patent at 5:16-17 (noting that blocks in a "spare good block table" are used to replace defective blocks). According to IMS, this use of spare blocks is the claimed "adjust[ment]" or "adapt[ing]" of the "correspondence of blocks to zones." *See* Ex. 4 ¶ 167.

Critically, there is no dispute that the spare blocks stored in the '507 patent's "spare good block table" lack logical addresses and are not addressable by the host, *i.e.*, they are not "assigned blocks." *See, e.g.,* Ex. 7 ¶ 33 [redacted] *see also* Ex. 6 at 119:4-22 (spare block pool is not a logical zone); 202:21-14 (noting that the logical address is "removed" before replacement occurs). This "spare block table" is like the "redundant" block zone of Tanaka, both of which include blocks with no logical addresses (no "assigned blocks") and is the very type of block that IMS said in its Federal Circuit briefing cannot satisfy the claim. Ex. 13, at 41 (distinguishing Tanaka because "Tanaka's redundant blocks have no logical addresses assigned to them"). Thus, IMS cannot show that the MX500 meets the requirement that "the controller can adjust zone boundaries such that ***assigned blocks*** from one logical zone are shifted to another logical zone," because any alleged adjustment involves shifting an ***unassigned*** block. Moreover, because they lack logical addresses when they are moved, the spare blocks are not "from" any logical zone. *See, e.g.*, Ex. 14, at 2 (stating that "if none of the blocks" in a "block area is assigned a logical address, it is not a zone as required by the claim"); 9 (noting that blocks are not assigned addresses that are part of a logical zone if they are not "included in any address translation table").

IMS also cannot prove that the P320h and P420m products infringe under the Court's claim construction. [redacted]

B. IMS's Infringement Claims Are Inconsistent With Its Past Representations Regarding The '498 Patent

Although IMS agrees that in all of the accused products, [redacted] it nonetheless argues that Micron's products can still infringe because "[n]othing in the claims, claim construction, or any prior ruling requires that [redacted]" Ex. 7 ¶ 33. IMS is wrong. It is "assigned blocks" (*i.e.*, blocks with a logical address) that must be shifted. Moreover, the shifted blocks must be "from one logical zone" at the time they are moved to "another" zone. IMS itself has repeatedly characterized the '498 patent this way. Indeed, IMS has even explained that "adjusting blocks that are not yet assigned to logical zones is not enough to satisfy the claim limitations." Ex. 14 at 2. Similarly, IMS explained that "unless they are

already assigned or mapped to logical addresses," blocks "are not 'already assigned for address translation' as required." *Id.* at 6. IMS presumably took this position because this is all that the '498 patent discloses: in all cases, blocks that currently have logical addresses are moved from one logical zone to another. *See* '498 patent at Fig. 6, 11:22-34 (depicting and discussing the shifting of blocks from one logical zone to another: the blocks have logical addresses before, during, and after the shift). The patent makes no mention of blocks passing through an addressless "intermediate" state.

IMS may also attempt to argue that the prior art it distinguished during IPR is different than Micron's products. In that prior art, the shifted blocks were part of a spare pool and thus never had logical addresses. But that is of no moment. IMS repeatedly and consistently argued to the PTAB and the Federal Circuit that the claims require the movement of "assigned blocks" (*i.e.*, blocks with logical addresses) "from" one logical zone to another. *See, e.g.,* Ex. 14 at 2 ("the claim[s] require[] that the controller can adjust zone boundaries by shifting blocks from one logical zone to another logical zone."). IMS did not argue to the Federal Circuit or the Board that the '498 patent's claims only exclude the use of blocks that have never had logical addresses. It is blackletter law that claims are interpreted based on what a patentee actually said to distinguish prior art, not on an after the fact determination of the minimum argument that theoretically may have sufficed to distinguish the art. *See, e.g., Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 957 (Fed. Cir. 2000) (rejecting patentee's "request for a mulligan that would erase from the prosecution history the inventor's disavowal of a particular aspect of a claim term's meaning"); *see also Horizon Medicines LLC v. Alkem Labs., Ltd.*, No. 18-1014-RGA, 2020 WL 4569472, *3 (D. Del. Aug. 7, 2020) (rejecting patentee argument that

its claims should exclude only "the specific combination of elements presented by the prior art" and not the full extent of subject matter embraced by its prosecution statements).

Here, the Board, the Federal Circuit, and this Court have all relied on IMS's statements, and the cited portions of the '498 patent, to construe the claims. These statements and the Court's construction require that blocks have an assigned logical address and be from a logical zone when shifted. Because the Court's construction does not cover a block that is stripped of its logical address and becomes unassigned when it is shifted, Micron's products cannot infringe.

VI. MICRON IS ENTITLED TO PARTIAL SUMMARY JUDGMENT OF NO PRE-SUIT DAMAGES FOR THE '498 PATENT FOR FAILURE TO MARK.

Pursuant to 35 U.S.C. § 287(a), absent actual pre-suit notice to a defendant, a patentee who fails to mark its patented products cannot recover pre-suit damages from the defendant. IMS filed this case in December 2014. D.E. 1. It is undisputed that IMS did not provide Micron pre-suit notice of alleged infringement. Ex. 15 at 45:3-47:13. [redacted] Accordingly, if SanDisk, the original patentee, failed to mark products that embody the '498 patent, IMS cannot recover pre-suit damages. *Horatio Washington Depot Techs. LLC v. TOLMAR, Inc.*, No. CV 17-1086-LPS-CJB, 2019 WL 1276028, at *1-2 (D. Del. Mar. 20, 2019). Here, IMS cannot meet its marking burden.

As the party alleging failure to mark, Micron bore only an initial burden—a "low bar"—of identifying the products believed to be unmarked patented articles subject to the marking requirement. *Arctic Cat Inc. v. Bombardier Rec. Prods. Inc.*, 876 F.3d 1350, 1368 (Fed. Cir. 2017). Micron met this burden. Over a year ago, Micron's answer alleged that SanDisk products (microSD, iNAND, and Ultra e.MMC 4.41) embodied the '498 Asserted Claims. D.E. 162 ¶¶ 3-6. *See Packet Intelligence LLC v. NetScout Sys., Inc.*, 965 F.3d 1299, 1312 (Fed. Cir.

2020) (burden satisfied by "articulat[ing]" the unmarked products). Micron went further, citing evidence to illustrate that under IMS's asserted claim scope, these SanDisk products were likely to embody the Asserted Claims and that such products were sold in the U.S. Ex. 5 ¶¶ 132-40.

Because Micron met its burden, IMS was required to show that the identified products do not embody the Asserted Claims with "counter-evidence." *See Biedermann Techs. GmbH & Co. KG v. K2M, Inc.*, 528 F. Supp. 3d 407, 420-423 (E.D. Va. 2021). During the litigation, IMS had every opportunity to develop such evidence, because IMS's patent purchase agreement with SanDisk gave IMS the right to request assistance from SanDisk. Ex. 16, § 4.4. Nonetheless, IMS has failed to show that SanDisk's products do not practice the claimed inventions. At his deposition, IMS's expert, Dr. Wolfe, stated that he did not know whether the SanDisk products embodied the asserted '498 claims. Ex. 6 at 94:3-5, 210:6-15. This is not evidence of SanDisk's non-use. Nor has IMS produced any other evidence showing that SanDisk's products did not practice the Asserted Claims. In his expert report, Dr. Wolfe opined only that ***Micron's proffered evidence*** is not enough to show that the SanDisk product are embodying or were sold in the U.S. Ex. 7 ¶¶ 40-42. But that opinion is beside the point: the test is not whether Micron proved that SanDisk's products embody the patent, but whether IMS produced evidence that they do not. IMS has failed to meet its burden. *WiAV Solutions LLC v. Motorola, Inc.*, 732 F. Supp. 2d 634, 640 (E.D. Va. 2010) (granting summary judgment where, among other things, patentee's only relevant witness "could not say whether or not the [products] practiced the Patent").

VII. [redacted]

[redacted]

VIII. [redacted]

[redacted]

[redacted]

[redacted]

IX. CONCLUSION

For the foregoing reasons, Micron's motions for summary judgment and partial summary judgment should be granted.

sold also provide data on which entity shipped the product. IMS did not use this information to calculate damages for Micron's alleged infringement as distinct from acts of its subsidiaries.

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CERTIFICATE OF SERVICE

I hereby certify that on March 25, 2022, true and correct copies of the foregoing document were caused to be served upon the following counsel via electronic mail:

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